Techniques for Estimating the Effect of Combinatorial SER at the Chip Level

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Outline

- Are SETs Relevant?
- State of the Art
- Cell Level SET Characterization
- Proposed SoC Analysis Technique
- Simulation Results
- Conclusions and Future Work
Are SETs Relevant?
Setting the Context

- Problem
  - Soft error analysis of SoCs
  - Determination of contribution from SETs

- Application domain
  - Terrestrial applications
  - Recent process technologies (<=28nm)
  - Large SoCs (100M+ logic gates)
  - Moderate frequencies (600MHz..1000MHz)

- Relevant
  - Contribution of SETs comparable to error bars of the effective SER analysis (say 10..15%)
SETs: Review of Masking Effects

Logical Masking

- Depends on input vectors!

Electrical Masking

- Depends on routing/wiring

Temporal / Latch Window Masking

- Depends on distribution of pulse widths

\[ TDR = \frac{PW}{TCLK} \]
Industry Design Trends

Memory SER
250+ Mbits

FF SER
5..20 MFFs

Combo SER
50..200 MGates

Data Lifetime (2-5x)
TDR, AVF (10-50x)
TDR, LDR, EDR, AVF (1000x)

Selective use of HFF is becoming common
Adjacent bit ECC becoming common
De-Rating
Interleave + ECCs (10000x)
Selective HFF (~5-10x)
No Mitigation

De-Rated SER
Effective

Selective use of HFF is becoming common
State of the Art in SET Estimation
Many system/fabless companies perform SEU analysis using Excel. Typically one line devoted to estimating SETs using:
- Total # of combo gates
- Single, global FIT rate number
- Single, global de-rating number

<table>
<thead>
<tr>
<th>Type</th>
<th>Number Gates (M)</th>
<th>Raw SET FIT (FIT/MBIT)</th>
<th>De-Rating</th>
<th>Effective Rate (FIT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Combo</td>
<td>124.5</td>
<td>325</td>
<td>0.002</td>
<td>80.9</td>
</tr>
</tbody>
</table>

Actual values are not representative, but spreadsheet format is typical.

De-rating values typically taken from published papers.
State of the Art - Research

  - SEAT-DA evaluates effect of neutrons and resulting charge deposition
  - SETA-LA uses pre-characterized models of pulse transfer through gates
  - Results for small circuits (ISCAS<1200 gates) compared with spice analysis

- **MARS-C** – Miskov-Zivanov – [DAC’10]
  - Unified analysis of TDR, LDR and EDR
  - Use BDDs and ADD to represent the sensitive path to the outputs
  - Results presented for ISCAS, MCNC benchmarks, compared with spice analysis

- **HSEET** – Ramakrishnan – [ISQED’06]
  - Decomposition into basic blocks
  - Blocks characterized using SEAT-LA for intrinsic SER and propagation
  - Results presented for small circuits (<2000 gates)

- **GLASSEE/ROBAN** - Alexandrescu – [LATW’02]
  - Optimized techniques for LDR+TRD using event-based simulator

- **Polian** – [ISVLSI’08]
  - Scalable, probabilistic approach for LDR (only) on large gate-level circuits
Cell Level SET Characterization
Test Chips vs. Simulation

- Observations subject to deformations (filtering/broadening)
- Limitations on minimum observed pulse width
- Small number of gate types are tested
- Gates are tested in a single (few) states: \( AB = \{ 00, 01, 10, 11 \} \)
- High confidence in observed results

- Large number of gates can be simulated (full cell library)
- All input states can be considered
- Observations are not “distorted”
- Requires calibration to build confidence

Test Chips vs. Simulation

- Broaden Data Set
- Calibration
- TCAD/SPICE - Type Simulation
TFIT Simulation Results – Alpha/Neutron

- Alpha sensitivity varies depending on gate types
- Alpha produce short transients
28nm Simulations : Multiple Gates

Combinatorial FIT By Gate Type per Pulse Width

Alpha and Neutron - 28nm Process

- SET FIT rates for different pulse widths
- Neutron and alpha contribution
- Obtained using IROC’s TFIT cell-level SER tool

Large variation based on gate-type

Short transients are dominant
Simulation Results – Voltage Effect

Combinatorial (Alpha+Neutron) FIT rate of INV Cell

- Voltage effect is well studied
- A +/-10% voltage change can introduce large >1.5x variation in SET rate
Simulation Results – Drive Strength

Combinatorial (Alpha+Neutron) FIT rate of INV Cell

(voltage = Nominal)

- Effect of cell drive strength is well studied
- Cells with largest drive strengths are nearly insensitive to SETs
Simulation Results – Drive Strength

But: the effect of drive strength is complex

In some cases, an increase in drive strength increases SET FIT
The sensitivity of a gate depends on the state of its inputs.

For a complex gate – the sensitivity can vary by a factor of 2x.
Proposed SoC Analysis Technique
Proposed Technique

- Exploits hierarchy and abstraction
  - Pure gate-level analysis not scalable
  - Starting from RTL enables early estimation
- Builds on a library of pre-analyzed cells and circuit blocks

Pre-Characterization

Circuit Analysis

High Level Blocks

Cell Library

RTL

LDR Lookup

Block Decomposition

Gate Estimation

Raw SET Estimation

TDR Estimation

De-Rated SET Rate

*
High Level Library Characterization

- Library model is simplified
- Sensitivities averaged by category and pulse width

<table>
<thead>
<tr>
<th>Cell Type</th>
<th>FIT PW&lt;50ps</th>
<th>FIT PW=50..75ps</th>
<th>FIT PW&gt;75ps</th>
</tr>
</thead>
<tbody>
<tr>
<td>INV/BUF</td>
<td>19</td>
<td>5</td>
<td>1</td>
</tr>
<tr>
<td>AND/NAND</td>
<td>42</td>
<td>15</td>
<td>3</td>
</tr>
<tr>
<td>OR/NOR</td>
<td>33</td>
<td>12</td>
<td>5</td>
</tr>
<tr>
<td>XOR/XNOR</td>
<td>109</td>
<td>59</td>
<td>6</td>
</tr>
<tr>
<td>Complex</td>
<td>147</td>
<td>65</td>
<td>39</td>
</tr>
</tbody>
</table>

Note: SET characteristics of complex gates quite different from inverters. Many test-chips extrapolate results from an inverter chain to full-chip....

Results on this slide are for NanGate 45nm cell library.
Combinatorial Blocks

- Adders, muxes, multipliers, encoders, CSRs,…
- Using fast fault injection[1] compute the:
  - Intrinsic LDR from gates in the circuit to an output
  - Propagation LDR from inputs to outputs
  - Consider uniform random input vectors

<table>
<thead>
<tr>
<th>Block</th>
<th>Cell Count</th>
<th>Intrinsic LDR</th>
<th>Propagation LDR</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-bit adder (CLA)</td>
<td>41</td>
<td>0.88</td>
<td>1.00</td>
</tr>
<tr>
<td>MUX 8:1</td>
<td>7</td>
<td>0.429</td>
<td>0.227</td>
</tr>
<tr>
<td>ECC decoder (32-bit)</td>
<td>165</td>
<td>0.778</td>
<td>0.921</td>
</tr>
<tr>
<td>Register Logic</td>
<td>642</td>
<td>0.478</td>
<td>0.260</td>
</tr>
</tbody>
</table>

Combining the Models

Intrinsic SET SER is looked up based on
- Pre-computed gate-type distribution
- Cell library characterization

Errors are propagated based on pre-computed LDR

\[
\text{SER}_{\text{Network}} = (\text{IntSER}_A \times \text{ErrProp}_B \times \text{ErrProp}_{D1}) + \\
(\text{IntSER}_A \times \text{ErrProp}_{C1} \times \text{ErrProp}_{D2}) + \\
(\text{IntSER}_B \times \text{ErrProp}_{D1}) + \\
(\text{IntSER}_C \times \text{ErrProp}_{D2}) + \\
(\text{IntSER}_D)
\]
Simulation Results
32-Bit Open RISC ALU

- ALU is ~1800 gates
- RTL was synthesized FLAT into Nangate 45nm library using DC
- 300MHz operation
“Golden” Fault Injection

- SET faults are injected on the outputs of gates (one fault per run)
- Pulse distribution respects per-gate PW profile
- Faults uniform temporally across the clock cycle
- 25K fault injections performed
- Random input vectors

Flat GLN with SDF
## Results

### Gate-Level Fault Injection Results

<table>
<thead>
<tr>
<th>Simulation Type</th>
<th>S+H Violation</th>
<th>Error</th>
<th>Effective FIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Zero Delay</td>
<td>85</td>
<td>28</td>
<td>0.61 mFIT</td>
</tr>
<tr>
<td>Delays (SDF)</td>
<td>45</td>
<td>45</td>
<td>0.73 mFIT</td>
</tr>
</tbody>
</table>

Good correlation!

- Predicted FIT using hierarchical RTL approach: 0.76 mFIT
- With SDF annotation – observed PW at D-inputs was ~1.5x wider than injected pulse width
Conclusions and Future Work
Extrapolating Results to SoC Level

- Proposed methodology has been integrated into a spreadsheet-based tool

- Assume a SoC with **100M combinatorial** gates running at **800MHz**

- Extrapolation of example circuit in NanGate Library to SoC level
  - $0.76 \text{ mFIT} \times 55555 \text{ (gate ratio)} \times 2.6 \text{ (freq ratio)} \Rightarrow 112 \text{ FIT}$

- Extrapolation of results for 28nm commercial library
  - SET FIT rate in the range of [200..1000] FITs

- **Further de-rating required**:
  - Not all SETs that reach a FF cause functional errors
  - Expect an additional $\approx 10x$ de-rating from propagation of SET FIT to observable effects
Conclusions and Future Work

- For large designs with strong ECC (memories) and hardened FFs contribution of SETs is becoming relevant (e.g. >10% of effective FIT rate)

- Quality tools are required to:
  1. Quickly assess the potential effect of SETs
  2. Accurately characterize SETs in combinatorial cells
  3. Accurately characterize masking effects and predict effective SoC, combinatorial FIT rates
Thank You!

Questions?
Backup Slides
SET Test Results - Intel[1]

- Test Chip
  - Implemented 32nm, planar test chip (0.75v, 0.9v)
  - Inverter chains (6 and 10 long)
  - 800MHz..2GHz

- Test Chip Observations
  - Combo SER – increases linearly with clock frequency
  - Combo SER ≈ 0.6% of standard latch SER (0.75v, 1GHz)

- Simulation / Extrapolation
  - TIDSET spice simulator : time slices + spice simulation
    - Limited to small circuits
  - Extrapolation based on fanin and frequency
    - Upper bound : assuming LDRcomb=1
    - Combo SER <= 30% standard latch SER

Cell Level Simulation - TFIT

- Combinatorial SER simulations run on commercial 28nm cell library

- Performed using TFIT\(^1\)
  - Process technology characterized: one time TCAD simulations
  - SET sensitivity of cells evaluated using SPICE by injecting appropriate current pulses in each XTOR
  - Distribution of current pulses for neutrons defined by nuclear database and materials interactions

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\(^{1}\) Belhaddad, Perez, Nicolaidis, “Circuit Simulation of SEU and SET Disruptions by Means of an Empirical Model…”, RADECS’06.