Combined SER of Bulk 28nm Technology from Logic and Flip Flops

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Role of Frequency and Technology Scaling

- Past predictions suggested that logic upsets would dominate chip-level SER with frequency and technology scaling.

- Early predictions about logic upsets dominating chip level SER with technology scaling [2]

1. Buchner et al., IEEE TNS 1997
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- Logic upsets are linearly dependent on frequency
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- Cross-over/ threshold frequency is important
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  - Operating freq > threshold freq: logic upsets dominate SER
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- Hardening logic: Lower slope with frequency; higher cross-over frequency

For modern high-speed circuits, hardening strategy needs to be based on cross-over frequency of the design
32 nm CMOS Planar Technology

- Results at 32 nm node (Intel) investigated the contribution of logic upsets to the overall error rate

SET contribution of each gate in the logic block feeding a latch is less than 3% of the total errors at 32 nm

Gill et al., IEEE IRPS 2009
Total errors = Errors due to SETs + Errors due to SEUs

If total errors (SEU+SET) in a circuit and SEU errors are known, errors due to combinational logic can be estimated.
Flip-Flop and Logic Cross-Sections

Flip-flop Cross-section = Total Errors/ (Fluence x Number of FF)

Total Cross-section = (SEUs + latched SETs)/ (Fluence x Number of FF)

Logic X-section / stage = Total X-section – FF X-section
CREST$^1$ for FF Cross-Section

- The circuit was designed and fabricated at 40 nm and 28 nm TSMC bulk CMOS technology
- For the above structure, cross-section was evaluated per Flip-Flop

The logic block consisted of 72 inverters
Errors due to SET and SEU are propagated through the shift register

After Ahlbin J. et al Combinational Circuit for Radiation Effects Self-Test (C-CREST), IEEE TNS Dec 2008
Experimental Details

- Alpha particle exposures carried out using:
  - 5 MeV Americium-241 alpha source with activity of 10 μCi
  - Distance between alpha source and die ≈ 0.3 cm

- Chips were subjected to alpha-irradiation for at least 12 hours at each data point

- Clock frequency was varied up to 1 GHz
Flip-flop errors are largely independent of frequency.

Logic errors (latched SETs) are frequency dependent.

Flip-flop cross-section is 2X logic cross-section at 1 GHz.

- SEU contribution per FF
- SET contribution from a single logic block to a single FF
Low frequency cross-section for Alpha particles is dominated by FF SER

Logic CS increases from $4.5 \times 10^{-11} \text{ cm}^{-2}$ at 10 MHz to $7.5 \times 10^{-11} \text{ cm}^{-2}$ at 500 MHz
Supply voltage has little effect on the slope of Logic SER vs Frequency

Total error rate at 0.8 V, 125 MHz = error rate at 0.85 V, 480 MHz
Power & SER : VDD, F dependence

\[ \text{dynamic power} = 0.5CV^2F \]

\[ \text{SER}_{\text{latches}} = e^{Q_{\text{crit}}} \]

\[ Q_{\text{crit}} = f(CV \text{ and restoring current}) \]

\[ \text{SER}_{\text{logic}} = f(V, F) \]

- SER goals may be met by changing supply voltage and frequency
- Exploring reliability aware design for low power
Logic block consisted of a 4-bit digital comparator

Inputs on the 4-bit comparator were varied to estimate effects of logical masking on SER
Effects of Logical Masking (40 nm Node)

- Logical masking decreases the soft error cross-section
- Flip-flop cross-section is between 2X - 8X times the logic cross-section at 1 GHz
SETs from the comparator contribute about 35% of errors on a (D flip-flop + logic block C-CREST block)

For average combinational circuits, logic errors may dominate the SER in GHz range for this technology
Implications of Latch Design Hardness

- To observe effects of latch hardening on the cross-over freq, a C-CREST circuit with hardened latches was designed.
- The logic block consisted of a comparator (same as before).

![Diagram of the circuit with latches and comparators connected in series.]
Implications of Latch Design hardness (40 nm)

- At about 1 GHz the number of SET errors nearly equal SEUs for hardened latches
- With hardened latches, the cross-over frequency is lower
Summary

- FF SER are decreasing with scaling and are mostly independent of frequency.
- Logic SER increases linearly with frequency and slope of SER vs frequency decreases with scaling.
- Any bulk CMOS design with ~20 logic gates feeding into a FF will yield comparable logic SER and FF SER at 28 nm node around 1 GHz.
- Circuits operating at multi-GHz range of frequencies will have logic SER dominate over FF SER.